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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

NADAV, ORI

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/305,240

Applicant(s)

SHIM ET AL.

Examiner

ori nadav

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 25 October 2002.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-7 and 9 is/are pending in the application.

4a) Of the above claim(s) 1-4 is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 5-7 and 9 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s). _____.
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) Notice of Informal Patent Application (PTO-152)
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. 6) Other:

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DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 5-7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Subramanian et al. (5,668,021) in view of Applicant Admitted Prior Art (AAPA). Subramanian et al. teach in figure 7 and related text a transistor comprising: a semiconductor substrate 10 of a first conductivity type; source and drain regions 28, 30, 34, 36 of a second conductivity type formed in the substrate and defining between them a channel region, an impurity implantation region 24 of impurities of a second conductivity type (column 3, lines 56-58) formed in a first sector of the channel region, the first sector (i.e. the region where the impurity implantation region 24 is located) not reaching either one of the source region and the drain region 28, 30, 34, 36, the impurity implantation region of the first sector comprising a surface region of the second conductivity type, a second sector of the channel region exclusive of the first sector comprising a uniform doping concentration of the first conductivity type and a surface region of the first conductivity type, a gate insulating layer 12 on the substrate

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over at least a portion of the surface region of the first sector and the surface region of the second sector, and a gate 46 (14, 26 and 38, see column 5, lines 57-60) on the gate insulating layer over at least a portion of the first sector and over at least a portion of the second sector.

Although Subramanian et al. do not state that the second sector of the channel region comprises a uniform doping concentration, the embodiment of figure 7 does not recite any additional channel doping in the second sector (the second sector is a region in the channel region which is exclusive of the first sector) and no special substrate doping. Note that the second sector of the channel region is part of the substrate. Thus, the doping concentration of the substrate 10 is uniform, as claimed.

Subramanian et al. do not teach using the transistor as a pull up transistor, wherein one of the source and drain regions being electrically coupled to an I/O pad and the other one being electrically coupled to a Vdd terminal, and does not state that the impurity implantation region of the first sector is operable as a depletion channel, and the second sector of the channel region is operable as an enhancement channel.

AAPA teaches in figure 1 and related text (page 2, lines 1-15) a pull up transistor B, wherein one of the source and drain regions being electrically coupled to an I/O pad 20 and the other one being electrically coupled to a Vdd terminal.

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It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Subramanian et al.'s transistor as a pull up transistor, wherein one of the source and drain regions being electrically coupled to an I/O pad and the other one being electrically coupled to a Vdd terminal, as taught by AAPA, in order to use the device in an application which requires a pull up transistor. Note that in order to operate a pull up transistor one of the source and drain regions must be electrically coupled to an I/O pad and the other one must electrically coupled to a Vdd terminal. The combination is motivated by the teachings of AAPA who point out the need for an improved pull up transistor.

Furthermore, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). In this case, Subramanian's transistor is capable of performing as a pull up transistor.

Regarding the claimed limitations of an impurity implantation region of the first sector being operable under field effect as a depletion channel, and the second sector of the channel region being operable under field effect as an enhancement channel, although Subramanian et al. and AAPA do not state that the impurity implantation region of the first sector is operable under field effect as a depletion channel, and the second sector

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of the channel region is operable under field effect as an enhancement channel, these features are inherent in Subramanian et al. and AAPA's device for the following reasons. The first sector comprises first conductive type dopants and the second sector comprises second conductive type dopants. The equivalent circuit for Subramanian et al. and AAPA's transistor is identical to the equivalent circuit for applicant's transistor depicted in applicant's figure 7c. The equivalent circuit comprises three transistors operating at two different modes, a first sector operates at an n-channel (Subramanian et al., column 3, lines 59-61) as a depletion transistor, and a second sector operates at a p-channel as an enhancement transistor. Therefore, while operating the transistor as a pull up transistor, the impurity implantation region of the first sector of Subramanian et al. and AAPA's transistor is operable under field effect as a depletion channel (due to the first conductive type dopants), and the second sector of the channel region is operable under field effect as an enhancement channel (due to the second conductive type dopants), as claimed.

In the alternative, *regarding the claimed limitations of an impurity implantation region of the first sector being as a depletion channel, and the second sector of the channel region being as an enhancement channel, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function.* *In re Danley*, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does ."(emphasis in original) *Hewlett - Packard Co . v. Bausch & Lomb Inc .*

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15 USPQ2d 1525, 1528 (Fed. Cir. 1990). A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). In this case, the claimed structure is not distinct from prior art's structure, because Subramanian et al. and AAPA's transistor is identical to applicant's transistor.

Regarding claim 6, Subramanian et al. teach in figure 7 and related text a first sector 24 having a narrower line width than a line width of the gate 46 (14, 26 and 38, see column 5, lines 57-60).

Regarding claim 7, Subramanian et al. teach in figure 7 and related text a gate 46 (14, 26 and 38, see column 5, lines 57-60) comprises a first portion over the first sector and a second portion over the second sector; and the first portion is in a predetermined ratio with respect to the second portion.

Regarding claim 9, Subramanian et al. teach in figure 7 and related text a first sector separated from the source region and from the drain region by substantially equal distances (column 2, lines 45-47).

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Response to Arguments

3. Applicant argues on pages 3 and 4 that Subramanian et al. teach a buried junction 24, and thus not having a surface region as a depletion channel.

Figure 7 of Subramanian et al. depicts the top of region 24 being in direct contact with the surface of the substrate. Therefore, "buried junction 24" has a surface region, not spaced away from the surface of the substrate, as a depletion channel.

4. Applicant argues on pages 4 and 5 that Subramanian et al.'s device can not function as a pull up transistor, because the separation distance between the two regions is only 300-1000 Å.

Applicant merely speculates that the separation distance between the two regions is too small for Subramanian et al.'s device to operate as a pull up transistor. There is no evidence that Subramanian et al.'s device can not function as a pull up transistor.

5. Applicant argues on page 6 that AAPA is not prior art, because AAPA describes applicant's opinion of the need to improve pull ups transistors.

AAPA describes the disadvantages of prior art's device. The disadvantages of prior art's device are not part of the present invention, and thus can be used by an artisan to improve Subramanian et al.

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Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722

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and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is (703) 308-8138. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is 308-0956



TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Ori Nadav

December 30, 2002